Aaron C. Lindsay

Raleigh, NC

Summary

Software engineer and processor architect with strong experience methodically debugging challenging problems, distilling them down to their core, and developing robust solutions optimized for performance.

Expertise

Languages: Assembly (ARM), (Ba)sh, C, C++, Go, HTML/CSS, JavaScript, make, Python, (reading) verilog
Skills: Design/develop/debug applications, libraries, and operating system kernels (Linux), optimize for performance (from processor microarchitecture to assembly to web applications), construct software CPU models, debug complex multi-system problems, Linux/Unix administration, automation, data analysis

Experience

Ampere Principal Architect August 2018 to present

- Modeled performance of next-generation CPU design, allowing accurate performance projections
- Uncovered/prevented performance and functional defects through performance validation of RTL/verilog design and (micro)architectural study
- Proposed and studied feasibility and efficiency of potential CPU microarchitectural features
- Designed and implemented methodology to collect workloads for processor performance model using QEMU, also contributing to upstream development of its plugin interface
- Conceived of and implemented technology to collect identical sections of workload execution in different formats to allow performance validation across simulation platforms

Qualcomm Senior Engineer August 2012 to August 2018

- Developed lightweight containers, Python workloads API, and `ptrace`-based tools to accelerate data-gathering and analysis for software and hardware optimization by enabling automated profiling across arbitrary workloads
- Maintained in-house Linux distribution, authoring kernel patches and custom packaging to support modeling
- Debugged Linux kernel and application functionality and performance at all levels – from high-level software using `gdb` to custom model instruction traces and processor pipeline interactions
- Supported mapping performance data from software processor models to benchmark source code symbols by adding semihosting support for perf events in the Linux kernel
- Influenced next-generation processor design via micro-benchmarks and innovative workload sampling methods, reducing the required performance model runtime over 1000×
- Pioneered basic block vector validation for model workloads, ensuring trusted results for critical microarchitectural decisions – achieved correlation error of only 1% between software models and silicon
- Adapted open-source software to speed up workload creation and contributed changes upstream, including emulated ARM PMUv3 (performance monitor) for QEMU

Real-time Systems Research at Virginia Tech August 2010 to May 2012

- Formulated and empirically evaluated cache-aware real-time scheduling algorithms and partitioning schemes
- Developed and maintained ChronOS Linux, a set of Linux kernel scheduling patches and library/test applications

Qualcomm Software Development Engineer Summer 2011

- Implemented snapshot/restore and fast-forwarding mechanisms for next-generation mobile processor simulator

IBM Emerging Technologies (jStart Team) January 2009 to February 2010

- Developed distributed mashup technology with Java and JavaScript (granted patent US20110161833)

Technical Hobbies

- Develop open-source software – recently personal finance/accounting software in python, Go, and ReactJS
- Administer web services for family/friends using Ansible, including email, wiki, personal cloud, and git

Education

Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA

M.S. Computer Science and Applications (3.95/4.0 GPA) June 2012
Thesis: *LWFG: A Cache-Aware Multi-core Real-Time Scheduling Algorithm*

B.S. Computer Science / Math Minor (Summa Cum Laude - 3.90/4.0 GPA) December 2010